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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/717,292	11/18/2003	Thomas Mohr	10191/3361	7553

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EXAMINER	
AMAYA, CARLOS DAVID	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/717,292	MOHR ET AL.	
	Examiner	Art Unit	
	Carlos Amaya	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/18/2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/18/03,07/18/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figures 1 and 2 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. With respect to figure 5 on the specification Applicant refers to a pulse duty factor 19, but in the figures there is no reference character 19. Instead there is a reference number 49.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

4. Claims 1,3-6 are rejected under 35 U.S.C. 102(a) as being anticipate by (Fumiaki JP 2003 259634).

With respect to claim 1 Fumiaki discloses a method for activating a number n of electrical loads in a circuit assemblage, n being at least 2, the method comprising: activating the n electrical loads by n pulse width modulated signals (Paragraph 0001), wherein for the activating of the n electrical loads, the n pulse width modulated signals are generated in a time-offset so that an effective value of a direct current flowing in a supply lead to the n electrical loads is reduced (Paragraph 0012, the invention uses a delay circuit to provide the time-offset of the signal generated by the microcontroller 3 to supply the loads, see figure 2).

With respect to claim 3 Fumiaki discloses the method of claim 1, wherein the time offset between the n pulse width modulated signals equals an nth part of a period of the pulse width modulated signals (Figure 2 shows that the time offset toff is part of one period ts).

With respect to claim 4 Fumiaki discloses the method of claim 1, wherein the n electrical loads are activated with the n pulse width modulated signals at a pulse duty factor of 1/N. The duty factor in Fumiaki invention is controlled by the delay circuit, so that the PWM signals that control the loads do not overlap mutually, thus the duty factor can be adjusted depending on the number of loads and the delay circuit.

With respect to claim 5 Fumiaki discloses the method of claim 1, wherein at a pulse duty factor of 1/N, the direct current, which is reduced by half as compared to an amplitude of a maximally permissible current, is generated in the supply lead to an electrical system of a motor vehicle. Figure 2 shows PWM control signals ps1 and ps2

that control the power supply to the load, with their respective time offset, depending on the duty cycle of the signals supply to the load, Paragraph 0012.

With respect to claim 6 Fumiaki discloses the method of claim 1, wherein the n electrical loads are activated by power semiconductor components respectively associated with them, each of which has associated with it a separate activation line for transmission of the pulse width modulated signals. Figure 1 shows the PWM signals applied to transistors 12a and 12b, by signals ps1 and ps2 to control the power supplied to the loads by controlling the FET 11a and 11b and the power applied to the loads.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2,7-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over (Fumiaki JP 2003 259634) in view of Admitted prior art.

With respect to claim 2 Fumiaki in view of Admitted prior art discloses the method of claim 1, Fumiaki, however, does not disclose expressly that a filter for influencing electromagnetic compatibility is placed upstream from the n electrical loads.

Applicants admitted prior art discloses an EMC 3 composed of a filtering arrangement having an inductor and a capacitance.

It would have been obvious to a person of ordinary skill in the art at time the invention was made to add the filtering arrangement disclosed by the applicant in the invention disclosed by Fumiaki.

The suggestion or motivation for doing so would have been to provide a system, which is not disrupted due to the signals applied to the switches. The filter provides protection against high rises of the current provided to the load, and prevents overloading of the electrical system.

With respect to claim 7 Fumiaki in view of Admitted prior art discloses an apparatus for activating n electrical loads.

Fumiaki discloses a microcontroller (microcontroller 3) to activate the n electrical loads (LP1 and LP2) and to generate activation signals (ps1 and ps2), for providing time-offset energization of n power semiconductor components a microcontroller includes a first output (T1) and a second output (T2) to which a first activation line and a second activation line are connected for activating the n power semiconductor components of the n electrical loads (Signals are connected to switches 12a and 12b and to FET 11a and 11b respectively); wherein the apparatus activates the n electrical loads by n pulse width modulated signals (Figure 2 shows the signals being applied to the transistors as PWM signals), wherein for the activating of the n electrical loads, the n pulse width modulated signals are generated in a time-offset so that an effective value of a direct current flowing in a supply lead to the n electrical loads is reduced (Fumiaki discloses that a delay circuit is employ for avoiding the mutually overlap of PWM control

signals, thus it is understood that the power supply to the load is going to depend on the time offset, duty cycle, of the signal and the power is going to be reduced).

Fumiaki, however, does not disclose expressly a filter to influence electromagnetic compatibility, the filter including an inductance arrangement and a capacitance arrangement.

Applicants admitted prior art disclose a filter arrangement including an inductor and a capacitor as seen on the available circuit assemblage of figure 1. One of ordinary skill in the art would have envisioned adding a filter arrangement in Fumiaki's invention.

The suggestion or motivation for doing so would have been to provide a system, which is not disrupted due to the signals applied to the switches. The filter provides protection against high rises of the current provided to the load, and prevents overloading of the electrical system.

With respect to claim 8 Fumiaki in view of Admitted prior art discloses the apparatus of claim 7, wherein the n power semiconductor components include at least one of MOSFET transistors, bipolar transistors, IGBT transistors and IGCT transistors. Fumiaki discloses that the switches controlling the power being supplied to the load are FET 11a and 11b, one of ordinary skill in the art would have envisioned to use a suitable power semiconductor to provide the switching on and off.

With respect to claim 9 Fumiaki in view of Admitted prior art discloses the apparatus of claim 7, wherein a first electrical load and a second electrical load represents one of a double blower and a tandem blower, one of the electrical loads being associated with a radiator of an internal combustion engine and another of the

electrical loads being associated with a heat exchanger of a vehicle climate control system of a motor vehicle. It would have been obvious to one of ordinary skill in the art to connect a suitable load, as the loads disclosed by Fumiaki, which is dictated by the voltage source available and system requirements.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner's supervisor, Brian Sircus who can be reached on (571)272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CA

PHUONG T. VU
PRIMARY EXAMINER